HIGH SPEED, LOW POWER COMPARATOR

ABSTRACT OF THE DISCLOSURE

A method for reducing bit errors in an analog to digital converter having an array of comparators. The outputs of first and second comparators are received as in inputs to an Exclusive OR gate. The first and second comparators are separated in the array by a third comparator. The output of the Exclusive OR gate is used to determine if the third comparator is in a metastable condition. If the third comparator is in a metastable condition, the bias current of the latch circuit of the third comparator is increased to increase the rate at which the third comparator transitions to a steady state.